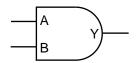
KX88 Digital Debug Prep Quiz

Note: If you get any questions wrong, or if you get them correct but really don't understand why, you will not be able to troubleshoot the KX88 Key Bank issues

1. Identify the logic gate:



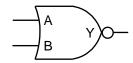
Circle one:

- A OR Gate
- B AND Gate
- C XOR Gate
- D NOR Gate
- E NAND Gate
- F XNOR Gate
- G INV Gate
- 2. Complete the Truth Table for the gate in Question 1:

Α	В	Υ
L	L	
L	Н	
Н	L	
Н	Н	

L = Low, H = High, X = Don't Care

3. Identify the logic gate:



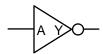
Circle one:

- A OR Gate
- **B** AND Gate
- C XOR Gate
- D NOR Gate
- E NAND Gate
- F XNOR Gate
- G INV Gate
- 4. Complete the Truth Table for the gate in Question 3:

Α	В	Υ
L	L	
L	I	
Н	L	
Н	I	

L = Low, H = High, X = Don't Care

5. Identify the logic gate:



Circle one:

- A OR Gate
- **B** AND Gate
- C XOR Gate
- D NOR Gate
- E NAND Gate
- F XNOR Gate
- G INV Gate
- 6. Complete the Truth Table for the gate in Question 5:

Α	Υ
L	
Н	

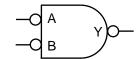
L = Low, H = High, X = Don't Care

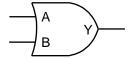
7. What is the proper name of the gate in Question 5?

Circle one:

- A Diverter
- B Diode
- C Director
- D Flip-Flop
- E Dotted Triangle
- F Inverter
- G Tri-State Buffer

8. Compete the Truth Tables for both of these gates:





Α	В	Υ
L	L	
L	Ι	
Н	L	
Н	Н	

Α	В	Υ
L	L	
L	Ι	
Н	L	
Н	Η	

L = Low, H = High, X = Don't Care

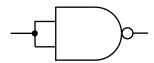
9. What is notable about these two gates in Question 8?

Circle one:

- A They have opposite logic outputs
- B They can both Tristate their outputs
- C They have an inverted output logic
- D There is nothing noteworthy other than being different gates
- E They use different power supplies
- F They can both act as inverters
- G They have identical logic
- 10. What is the theorem that is applied to the gates in Question 8?

- A Flip-Flip
- **B** Inversion
- C Differential
- D Pythagorean
- E De Morgan
- F Fundamental Theorem of Calculus
- G None

11. How is this gate being used?



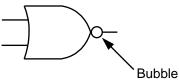
Circle one:

- A As a Tri-State Buffer
- B As an OR Gate
- C As an Inverter
- D It is improperly connected (inputs are shorted together)
- E As a Dotted AND Gate
- F As a Combiner
- G As a Diode
- 12. Draw the simplified symbol (if any), inside the dotted box below, for the gate in Question 11:

_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	- .	
I																													- 1	
ı																													- 1	
I																													- 1	
ı																													I	
ı																													- 1	
ı																													- 1	
ı																													I	
ı																													- 1	
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L	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_ 1	

Check here if the symbol is already simplified

13. What is the "Bubble" in the symbol below called?

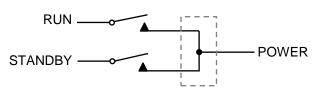


Circle one:

- A Bubble, that's it proper name
- B Flip-Flop
- C Donut
- D It has no name, just part of the symbol
- E State Indicator
- F Ring
- G Active High Output
- 14. What does the Bubble in Question 13 signify?

- A Temporary Output
- B Active High State
- C Active Low State
- D Tri-State Output
- E Bubble Logic
- F TTL Voltage Level
- G Ring Control

15. Identify the type of circuit used inside the dotted box:



Circle one:

- A Splitter
- B OR Gate
- C AND Gate
- D Splice
- E Wired-OR
- F Wired-AND
- G 3 Node Circuit

16. Identify this electronic component:



Circle one:

- A Inverter
- **B** Amplifier
- C Check Valve
- D Diode
- E Conductor
- F Transistor
- G Exclusive OR Gate
- 17. Identify the Cathode with a **K** and the Anode with an **A** next to its respective pin (inside the dotted boxes), and indicate the polarity (+ or -) inside each dotted circle:



18. Using two "methods" to follow circuitry, draw an arrow (inside the dotted boxes) to indicate which way current flows when the Diodes are forward biased (conducting):

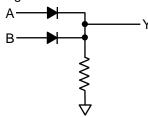
"Conventional Current"



"Electron Current"



19. Fill in the Truth Table and draw the Positive Logic and Negative Logic symbols in the dotted box below, that represents the following circuit:



Hint: Use Conventional Current Flow to fill in the following Truth Table, then determine which gate it is based on the logic results.

Α	В	Υ
L	L	
L	Η	
Н	L	
Н	Н	

L = Low, H = High, X = Don't Care

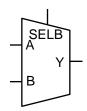
Draw the gates inside this box

Diaw the gates made this box	·
Positive Logic	Negative Logic

Extra Credit:

Above each Gate, write in its Type (**OR**, **AND**, **XOR**, **NOR**, **NAND**, **XNOR**, or **INV**). And also label each Pin Name (**A**, **B**, and **Y**)

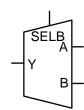
20. Identify this electronic component:



Circle one:

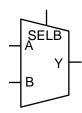
- A Combiner
- B Splitter
- C AND Gate Selector
- D Reverse Electronic Controlled SPDT Switch
- E De-Multiplexer
- F Multiplexer
- G OR Gate Selector

21. Identify this electronic component:



- A Combiner
- B Splitter
- C OR Gate Selector
- D Forward Electronic Controlled SPDT Switch
- E De-Multiplexer
- F Multiplexer
- G AND Gate Selector

22. Complete the Truth Table for the following component:



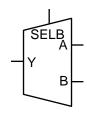
Note: The data sheet shows that Input A is selected when SELB is L and Input B is selected when SELB is H

Α	В	SELB	Υ
L	L	L	
L	Н	L	
Н	L	L	
Н	Н	L	
L	L	Н	
L	Н	Н	
Н	L	Н	
Н	Н	Н	

L = Low, H = High, X = Don't Care

Extra Credit:
Circle the Input States
that are actually Don't
Cares: X

24. Complete the Truth Table for the following component:



Note: The data sheet shows that Output A is selected when SELB is L and Output B is selected when SELB is H. The unselected output is forced to a L.

Υ	SELB	Α	В
L	L		
Н	L		
L	Н		
Н	Н		

Extra Credit:

Circle the Output States
that are actually forced to a
Low: L (unselected)

L = Low, H = High, X = Don't Care

23. The component in Question 22 is also known as a:

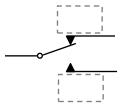
Circle one:

- A MUX
- **B DEMUX**
- C FF
- D AND
- E OR
- F SPDT
- G XOR

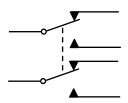
25. The component in Question 24 is also known as a:

- A MUX
- **B DEMUX**
- C FF
- D XNOR
- E AND
- F SPDT
- G OR

26. The following Switch is found to be "spring loaded" in its data sheet. It is designed to return to the position shown when not active. Indicate, in the dotted boxes, which positions are Normally Open (NO), Normally Closed (NC), or Normally Floating (NF):



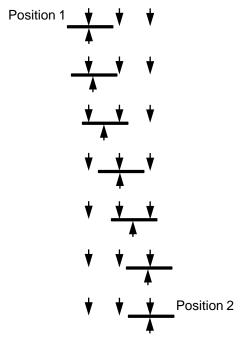
27. Identify this switch configuration:



Circle one:

- A 4P2T
- B SPST
- C SPDT
- D DPST
- E DPDT
- F 2-WAY
- G 4-WAY

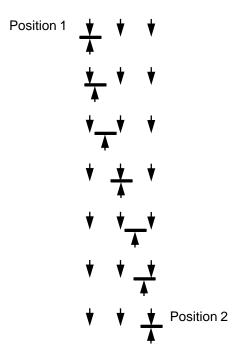
28. The following symbols explicitly show how a particular Slide Switch operates as it moves from Position 1 to Position 2. Identify this type of Switch:



- A Make Only
- B Break Only
- C Make Before Break
- D Break Before Make
- E Continuous Make
- F Continuous Break
- G Return To Make

KX88 Digital Debug Prep Quiz

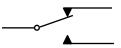
29. The following symbols explicitly show how a particular Slide Switch operates as it moves from Position 1 to Position 2. Identify this type of Switch:



Circle one:

- A Make Only
- B Break Only
- C Make Before Break
- D Break Before Make
- E Continuous Make
- F Continuous Break
- G Return To Break

30. As this Switch is drawn (not looking at its data sheet), what can be inferred about its operation?



Circle one:

- A Its contacts are Make Before Break (MBB)
- B Its contacts are Break Before Make (BBM)
- C It is Spring Loaded
- D It is a Rotary Switch
- E It is a Pushbutton Switch
- F It has a Center Off position
- G Its contacts are precise Pin Points

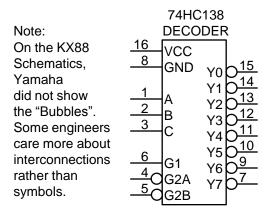
Prep for Question 31:

Dinon

How a 3 bit Binary Value represents a Decimal value

		Binary	<u> </u>	MSB: Most Significant Bit				
		Bits			st Significant Bit			
N	1SB		LSB					
	2	1	0	Decimal				
	0	0	0	0				
	0	0	1	1				
	0	1	0	2				
	0	1	1	3				
	1	0	0	4				
	1	0	1	5				
	1	1	0	6				
	1	1	1	7				

31. Complete the Truth Table for the following component:



If G1, G2A, or G2B are not satisfied, the device is "Disabled" and thus ALL outputs will be H regardless of the A, B, and C inputs. When inputs G1, G2A, and G2B are ALL satisfied, the device is "Enabled" and the outputs will be set according to inputs A, B, and C.

A, B, and C have a binary Value of 0 to 7. When Enabled, only the output that corresponds to that Value will go to the active state and the others will stay in the inactive state.

Example: G1=H, G2A=L, G2B=L C=L, B=H, A=L:

= LHL (logic levels on pins C B A respectively - binary)

= 010 (binary)

= 2 (decimal)

Thus, since it is Enabled, only the Y2 output will be active (low), the others will stay inactive (high).

Bin	ary Value L=0, H=1
MSB	LSB

Decimal Value

	MOR LOB														
	С	В	Α	G1	G2A	G2B	Decode	<u>Y0</u>	<u>Y1</u>	Y2	<u>Y3</u>	<u>Y4</u>	<u>Y5</u>	<u>Y6</u>	<u>Y7</u>
	Χ	Χ	Χ	L	Х	Х	Disabled	Н	Н	Н	Н	Н	Н	Н	Н
	Χ	Χ	Χ	Χ	Н	Х	Disabled	Н	Н	Н	Н	Н	Н	Н	Н
	Χ	Χ	Χ	Χ	Х	Н	Disabled	Н	Н	Н	Н	Н	Н	Н	Н
0	L	L	L	Н	L	L	Enabled								
1	L	L	Н	Н	L	L	Enabled								
2	L	Н	L	Η	L	L	Enabled	Н	Н	L	Η	Н	Н	Н	Н
3	L	Н	Н	Н	L	L	Enabled								
4	Н	L	L	Н	L	L	Enabled								
5	Н	L	Н	Н	L	L	Enabled								
6	Н	Н	L	Н	L	L	Enabled								
7	Н	Н	Н	Н	L	L	Enabled								
	1 2 3 4 5 6	C X X X X O L 1 L 2 L 3 L 4 H 5 H 6 H	C B X X X X X X O L L 1 L L 2 L H 3 L H 4 H L 5 H L 6 H H	C B A X X X X X X X X X X X X O L L L 1 L H 2 L H L 3 L H H 4 H L L 5 H L H 6 H H L	C B A G1 X X X X X X X X X X X X X X X X X X X X X X X X X X X X 1 L L H H 2 L H L H H 3 L H H H H 4 H L L H H 5 H L H H H 6 H H L H H	C B A G1 G2A X X X X X X X X X X X X X X X X X X X X 0 L L L H L	C B A G1 G2A G2B X X X X X X X X X X X H X X X X X H 0 L L L H L L 1 L L H H L L 2 L H L H L L 3 L H H H L L 4 H L L H L L 5 H L H H L L L 6 H H L H L L L	C B A G1 G2A G2B Decode X X X X X Disabled X X X X X H X Disabled X X X X X X H Disabled 0 L L L H L Enabled 1 L L H H L Enabled 2 L H H L Enabled 3 L H H L Enabled 4 H L L Enabled 5 H L H L Enabled 6 H H L H L Enabled	C B A G1 G2A G2B Decode Y0 X X X X X X Disabled H X X X X X X H Disabled H X X X X X X H Disabled H 0 L L L H L Enabled H 1 L L H H L Enabled H 2 L H H L Enabled H 3 L H H H L Enabled 4 H L H L Enabled 5 H L H L Enabled 6 H H L Enabled	C B A G1 G2A G2B Decode Y0 Y1 X X X X X X Disabled H H X X X X X X H Disabled H H 0 L L L H L Enabled H H 1 L L H H L Enabled H H H 2 L H H H L Enabled H H H 3 L H H H L Enabled Enabled H L Enabled H L Enabled H L Enabled H L Enabled Enabled H L Enabled Ena	C B A G1 G2A G2B Decode Y0 Y1 Y2 X X X X X X Disabled H L Inabled H H H H H L Inabled H H H H H L Inabled H H H H H H H	C B A G1 G2A G2B Decode Y0 Y1 Y2 Y3 X X X X X X Disabled H	C B A G1 G2A G2B Decode Y0 Y1 Y2 Y3 Y4 X X X X X X Disabled H	C B A G1 G2A G2B Decode Y0 Y1 Y2 Y3 Y4 Y5 X X X X X Disabled H <td>C B A G1 G2A G2B Decode Y0 Y1 Y2 Y3 Y4 Y5 Y6 X X X X X Disabled H</td>	C B A G1 G2A G2B Decode Y0 Y1 Y2 Y3 Y4 Y5 Y6 X X X X X Disabled H

L = Low, H = High, X = Don't Care

MSB: Most Significant Bit LSB: Least Significant Bit

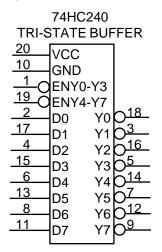
The "bar" (vinculum) over a Pin Name indicates an Active Low signal, for example:

Y2 is Active Low

Yellow is from the Example

KX88 Digital Debug Prep Quiz

32. Complete the Truth Table for the following component:



If ENY0-Y3 is not satisfied (inactive high), Outputs Y0 through Y3 will be Tri-State (disconnected). If ENY4-Y7 is not satisfied,

Outputs Y4 through Y7 will be Tri-State.

If ENY0-Y3 is satisfied (active low),

Outputs Y0 through Y3 will

follow their respective inputs but they will be inverted.

If ENY4-Y7 is satisfied, Outputs Y4 through Y7 will

follow their respective inputs but they will be inverted.

D0	D1	D2	D3	D4	D5	D6	D7	ENQ0-Q3	ENQ4-Q7	<u>V</u>	<u>Y1</u>	<u>Y2</u>	<u> </u>	<u>Y4</u>	<u>Y5</u>	<u>Y</u> 6	<u>77</u>
Х	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Н	Н		Т	Т		Т	Т	Т	
H or L	H or L	H or L	H or L	Χ	Χ	Χ	Χ	L	Н	D0		D2	D3	Т	Т		Т
Х	Χ	Χ	Χ	H or L	H or L	H or L	H or L	Н	L	Т	Т		Т	D4	D5		D7
H or L	L	L	<u></u> D0	D1	D2		D4		<u> </u> 6								

L = Low, H = High, X = Don't Care, T = Ţri-State

This means it follows the D0 input but is inverted

 $D0 = H \rightarrow Y0 = L$ $D0 = L \rightarrow Y0 = H$

Tri-State means the output is neither H or L, it is Hi-Impedance (like the output is disconnected).

Tri-Stating allows other ICs to drive signals that may share output pins on the same signals.